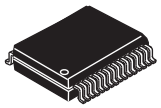
Document Number: MC33972
Rev. 19.0, 3/2012

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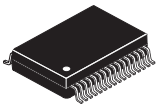
Multiple Switch Detection Interface with Suppressed Wake-up

33972/A/T

MULTIPLE SWITCH DETECTION INTERFACE



EW SUFFIX (Pb-FREE)
98ARH99137A
32-PIN SOICW



EK SUFFIX (Pb-FREE)
98ASA10556D
32-PIN SOICW EP

The 33972 Multiple Switch Detection Interface with suppressed wake-up is designed to detect the closing and opening of up to 22 switch contacts. The switch status, either open or closed, is transferred to the microprocessor unit (MCU) through a serial peripheral interface (SPI). The device also features a 22-to-1 analog multiplexer for reading inputs as analog. The analog input signal is buffered and provided on the AMUX output pin for the MCU to read.

The 33972 device has two modes of operation, Normal and Sleep. Normal mode allows programming of the device and supplies switch contacts with pull-up or pull-down current as it monitors switch change of state. The Sleep mode provides low quiescent current, which makes the 33972 ideal for automotive and industrial products requiring low sleep-state currents.

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33972TEW/R2	-40 °C to 125 °C	32 SOICW
MC33972ATEW/R2		
MC33972ATEK/R2		32 SOICW EP

Features

- Designed to operate 5.5 V ≤ V_{PWR} ≤ 26 V
- Switch input voltage range -14 V to V_{PWR}, 40 V Max
- Interfaces directly to MPU using 3.3 V/5.0 V SPI protocol
- Selectable wake-up on change of state
- Selectable wetting current (16 or 2.0 mA)
- 8 programmable inputs (switches to battery or ground)
- 14 switch-to-ground inputs
- Typical standby current - V_{PWR} = 100 μA and V_{DD} = 20 μA
- Active interrupt ($\overline{INT}$) on change-of-switch state

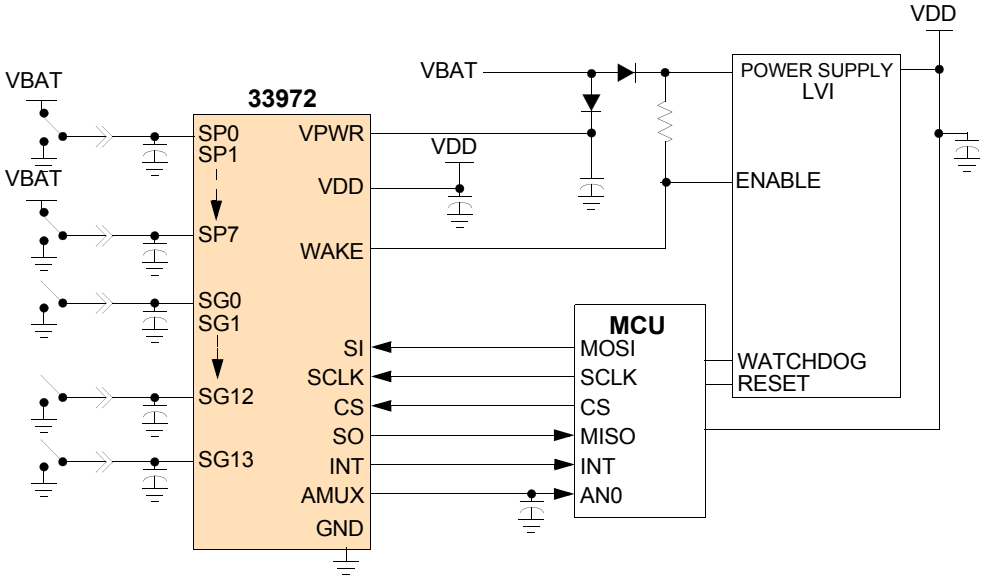


Figure 1. 33972 Simplified Application Diagram

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DEVICE VARIATIONS

Table 1. Device Variations

Device	Switch Input Voltage Range	Reference Location
33972	-14 to 38 V_{DC}	5, 6
33972A	-14 to 40 V_{DC}	5, 6

INTERNAL BLOCK DIAGRAM

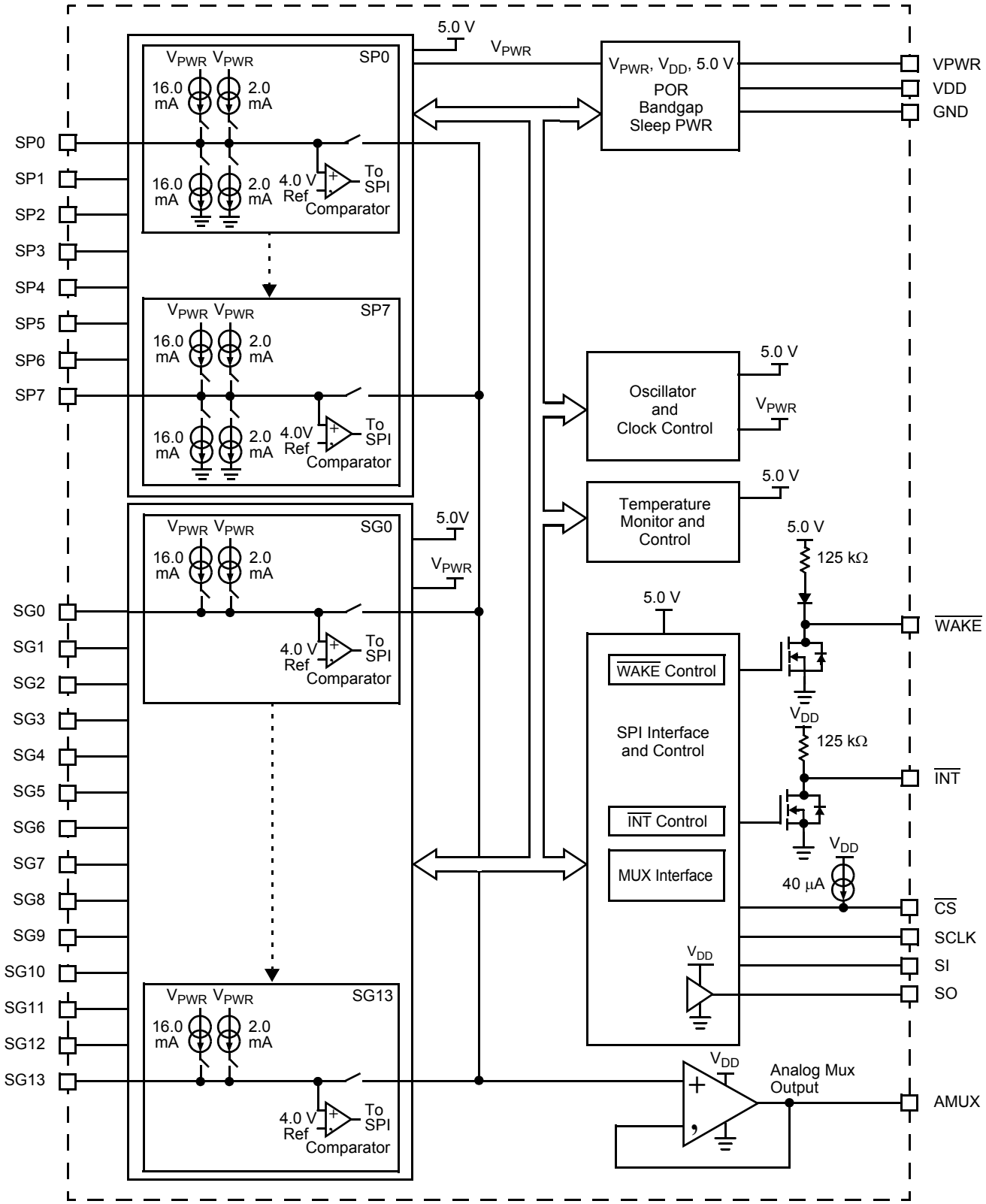


Figure 2. 33972 Simplified Internal Block Diagram

PIN CONNECTIONS

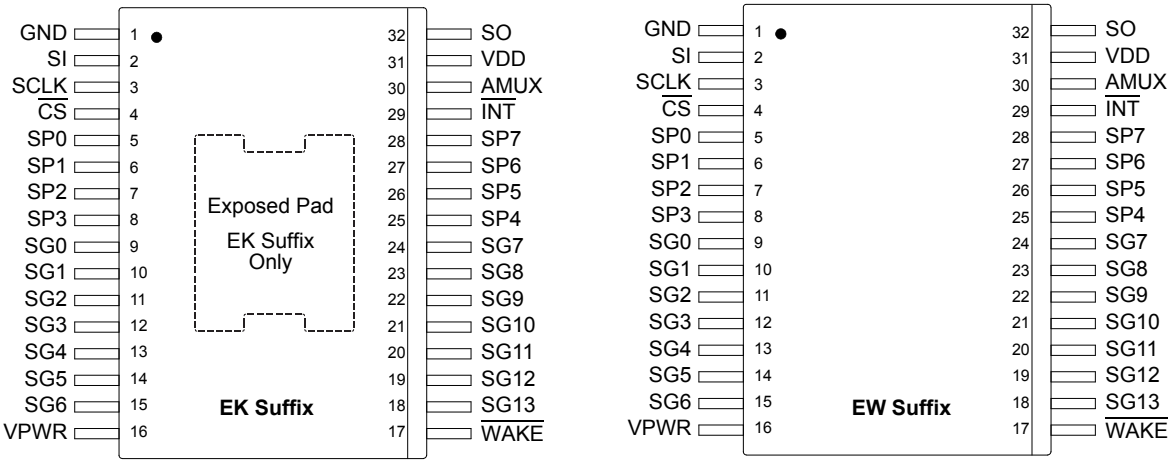


Figure 3. 33972 Pin Connections

Table 2. 33972 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 10.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	GND	Ground	Ground	Ground for logic, analog, and switch to battery inputs.
2	SI	Input	SPI Slave In	SPI control data input pin from the MCU to the 33972.
3	SCLK	Input	Serial Clock	SPI control clock input pin.
4	$\overline{CS}$	Input	Chip Select	SPI control chip select input pin from the MCU to the 33972. Logic [0} allows data to be transferred in.
5–8 25–28	SP0–3 SP4–7	Input	Programmable Switches 0–7	Programmable switch-to-battery or switch-to-ground input pins.
9–15, 18–24	SG0–6, SG13–7	Input	Switch-to-Ground Inputs 0–13	Switch-to-ground input pins.
16	VPWR	Input	Battery Input	Battery supply input pin. Pin requires external reverse battery protection.
17	$\overline{WAKE}$	Input/Output	Wake-up	Open drain wake-up output. Designed to control a power supply enable pin.
29	$\overline{INT}$	Input/Output	Interrupt	Open-drain output to MCU. Used to indicate an input switch change of state.
30	AMUX	Output	Analog Multiplex Output	Analog multiplex output.
31	VDD	Input	Voltage Drain Supply	3.3/5.0 V supply. Sets SPI communication level for the SO driver.
32	SO	Output	SPI Slave Out	Provides digital data from the 33972 to the MCU.
	EP	Ground	Exposed Pad	It is recommended that the exposed pad is terminated to GND (pin 1) and system ground, however, the device will perform as specified with the exposed pad unterminated (floating).

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
VDD Supply Voltage			V_{DC}
$\overline{CS}$, SI, SO, SCLK, $\overline{INT}$, AMUX[1]	–	-0.3 to 7.0	
$\overline{WAKE}$[1]	–	-0.3 to 40	V_{DC}
VPWR Supply Voltage[1]	–	-0.3 to 50	V_{DC}
VPWR Supply Voltage at -40 °C[1]	–	-0.3 to 45	V_{DC}
Switch Input Voltage Range	–	-14 to 40	V_{DC}
Frequency of SPI Operation (V_{DD} = 5.0 V)	–	6.0	MHz
ESD Voltage[3]			V
Human Body Model[2]	V_{ESD}	±2000	
Applies to all non-input pins		±2000	
Machine Model		±200	
Charge Device Model			
Corner Pins		750	
Interior Pins		500	
THERMAL RATINGS			
Operating Temperature			°C
Ambient	T_A	-40 to 125	
Junction	T_J	-40 to 150	
Storage Temperature	T_{STG}	-55 to 150	°C
Power Dissipation (T_A = 25 °C)[4]	P_D	1.7	W
Thermal Resistance			°C/W
Non-Exposed Pad			
Junction to Ambient	$R_{\theta JA}$	74	
Junction to Lead	$R_{\theta JL}$	25	
Exposed Pad			
Junction to Ambient	$R_{\theta JA}$	71	
Junction to Exposed Pad	$R_{\theta JC}$	1.2	
Peak Package Reflow Temperature During Reflow[5], [6]	T_{PPRT}	Note 6	°C

Notes

1. Exceeding these limits may cause malfunction or permanent damage to the device.
2. ESD data available upon request.
3. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
4. Maximum power dissipation at T_J = 150°C junction temperature with no heat sink used.
5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions 3.1 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{PWR} ≤ 16 V, -40 °C ≤ T_C ≤ 125 °C, unless otherwise noted.(7) Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Supply Voltage Range Quasi-functional(8) Fully Operational Supply Voltage Range Quasi-functional(8)	 $V_{PWR(QF)}$ $V_{PWR(FO)}$ $V_{PWR(QF)}$	 5.5 8.0 26	 – – –	 8.0 26 38/40	V
Supply Current All Switches Open, Normal Mode, Tri-state Disabled	$I_{PWR(ON)}$	–	2.0	4.0	mA
Sleep State Supply Current Scan Timer = 64 ms, Switches Open	$I_{PWR(SS)}$	40	70	100	µA
Logic Supply Voltage	V_{DD}	3.1	–	5.25	V
Logic Supply Current All Switches Open, Normal mode	I_{DD}	–	0.25	0.5	mA
Sleep State Logic Supply Current Scan Timer = 64 ms, Switches Open	$I_{DD(SS)}$	–	10	20	µA
SWITCH INPUT					
Pulse Wetting Current Switch-to-Battery (Current Sink)	I_{PULSE}	12	15	18	mA
Pulse Wetting Current Switch-to-Ground (Current Source)	I_{PULSE}	12	16	18	mA
Sustain Current Switch-to-Battery Input (Current Sink)	$I_{SUSTAIN}$	1.8	2.0	2.2	mA
Sustain Current Switch-to-Ground Input (Current Source)	$I_{SUSTAIN}$	1.8	2.0	2.2	mA
Sustain Current Matching Between Channels on Switch-to-Ground I/Os $\frac{I_{SUS(MAX)} - I_{SUS(MIN)}}{I_{SUS(MIN)}}$ X 100	I_{MATCH}	–	2.0	4.0	%
Input Offset Current When Selected as Analog	I_{OFFSET}	-2.0	1.4	2.0	µA
Input Offset Voltage When Selected as Analog $V_{(SP\&SGINPUTS)}$ to AMUX Output	V_{OFFSET}	-10	2.5	10	mV
Analog Operational Amplifier Output Voltage Sink 250 µA	V_{OL}	–	10	30	mV
Analog Operational Amplifier Output Voltage Source 250 µA	V_{OH}	V_{DD} -0.1	–	–	V
Switch Detection Threshold	V_{TH}	3.70	4.0	4.3	V
Switch Input Voltage Range 33972 33972A	V_{IN}	 -14 -14	 – –	 38 40	V
Temperature Monitor(9), (10)	T_{LIM}	155	–	185	°C
Temperature Monitor Hysteresis(10)	$T_{LIM(HYS)}$	5.0	10	15	°C

Notes
7. T_C is the T_{CASE} of the package
8. Device operational. Table parameters may be out of specification.
9. Thermal shutdown of 16 mA pull-up and pulldown current sources only. 2.0 mA current source/sink and all other functions remain active.
10. This parameter is guaranteed by design but is not production tested.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.1 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{PWR} ≤ 16 V, -40 °C ≤ T_C ≤ 125 °C, unless otherwise noted.(7) Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE					
Input Logic Voltage Thresholds(11)	$V_{INLOGIC}$	0.8	–	2.2	V
SCLK, SI, Tri-state SO Input Current 0 V to V_{DD}	I_{SCLK}, I_{SI}, $I_{SO(TRI)}$	-10	–	10	µA
$\overline{CS}$ Input Current $\overline{CS}$ = V_{DD}	$I_{\overline{CS}}$	-10	–	10	µA
$\overline{CS}$ Pull-up Current $\overline{CS}$ = 0 V	$I_{\overline{CS}}$	30	–	100	µA
SO High-state Output Voltage $I_{SO(HIGH)}$ = -200 µA	$V_{SO(HIGH)}$	V_{DD} -0.8	–	V_{DD}	V
SO Low-state Output Voltage $I_{SO(HIGH)}$ = 1.6mA	$V_{SO(LOW)}$	–	–	0.4	V
Input Capacitance on SCLK, SI, Tri-state SO(12)	C_{IN}	–	–	20	pF
$\overline{INT}$ Internal Pull-up Current	–	15	40	100	µA
$\overline{INT}$ Voltage $\overline{INT}$ = Open Circuit	$V_{\overline{INT}(HIGH)}$	V_{DD} -0.5	–	V_{DD}	V
$\overline{INT}$ Voltage $I_{\overline{INT}}$ = 1.0 mA	$V_{\overline{INT}(LOW)}$	–	0.2	0.4	V
$\overline{WAKE}$ Internal Pull-up Current	$I_{\overline{WAKE}(PU)}$	20	40	100	µA
$\overline{WAKE}$ Voltage $\overline{WAKE}$ = Open Circuit	$V_{\overline{WAKE}(HIGH)}$	4.0	4.3	5.3	V
$\overline{WAKE}$ Voltage $I_{\overline{WAKE}}$ = 1.0 mA	$V_{\overline{WAKE}(LOW)}$	–	0.2	0.4	V
$\overline{WAKE}$ Voltage Maximum Voltage Applied to $\overline{WAKE}$ Through External Pull-up	$V_{\overline{WAKE}(MAX)}$	–	–	40	V

Notes
11. Upper and lower logic threshold voltage levels apply to SI, $\overline{CS}$, and SCLK.
12. This parameter is guaranteed by design but is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.1 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{PWR} ≤ 16 V, -40 °C ≤ T_C ≤ 125 °C, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
SWITCH INPUT					
Pulse Wetting Current Time	$t_{PULSE(ON)}$	15	16	20	ms
Interrupt Delay Time Normal Mode	$t_{INT-DLY}$	– –	5.0 –	16 –	µs
Sleep Mode Switch Scan Time	t_{SCAN}	100	200	300	µs
Calibrated Scan Timer Accuracy Sleep Mode	$t_{SCAN\ TIMER}$	– –	– –	10 –	%
Calibrated Interrupt Timer Accuracy Sleep Mode	$t_{INT\ TIMER}$	– –	– –	10 –	%
DIGITAL INTERFACE TIMING[13]					
Required Low-state Duration on V_{PWR} for Reset[14] V_{PWR} ≤ 0.2 V	t_{RESET}	– –	– –	10 –	µs
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK Required Set-up Time	t_{LEAD}	100 –	– –	– –	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ Required Set-up Time	t_{LAG}	50 –	– –	– –	ns
SI to Falling Edge of SCLK Required Set-up Time	$t_{SI(SU)}$	16 –	– –	– –	ns
Falling Edge of SCLK to SI Required Hold Time	$t_{SI(HOLD)}$	20 –	– –	– –	ns
SI, $\overline{CS}$, SCLK Signal Rise Time[15]	$t_{R(SI)}$	–	5.0	–	ns
SI, $\overline{CS}$, SCLK Signal Fall Time[15]	$t_{F(SI)}$	–	5.0	–	ns
Time from Falling Edge of $\overline{CS}$ to SO Low-impedance[16]	$t_{SO(EN)}$	–	–	55	ns
Time from Rising Edge of $\overline{CS}$ to SO High-impedance[17]	$t_{SO(DIS)}$	–	–	55	ns
Time from Rising Edge of SCLK to SO Data Valid[18]	t_{VALID}	–	25	55	ns

Notes
13. These parameters are guaranteed by design. Production test equipment uses 4.16 MHz, 5.0 V SPI interface.
14. This parameter is guaranteed by design but not production tested.
15. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
16. Time required for valid output status data to be available on SO pin.
17. Time required for output states data to be terminated at SO pin.
18. Time required to obtain valid data out from SO following the rise of SCLK with 200 pF load.

TIMING DIAGRAMS

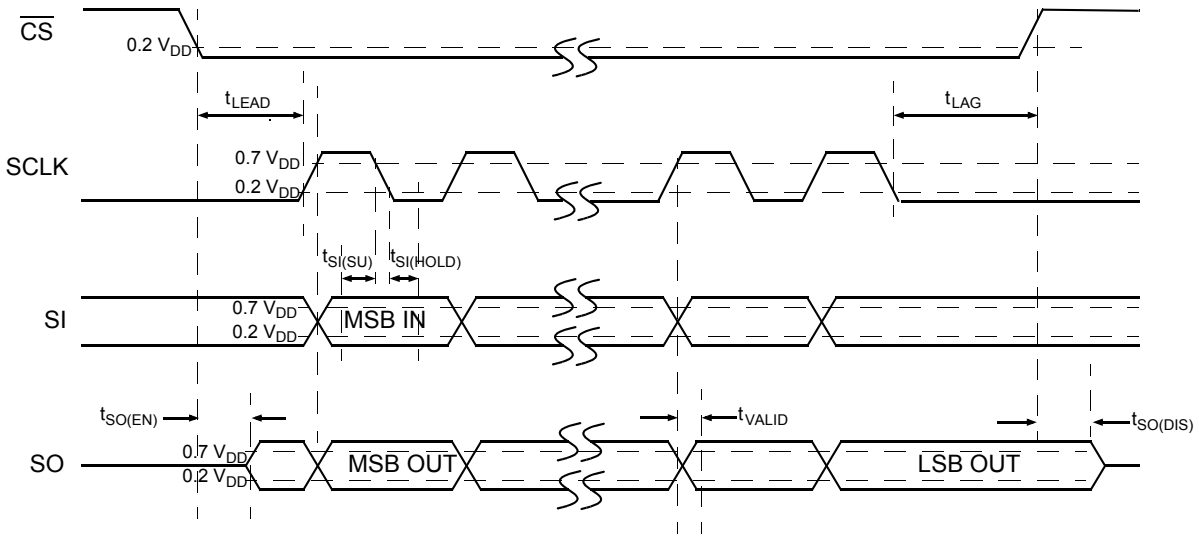


Figure 4. SPI Timing Characteristics

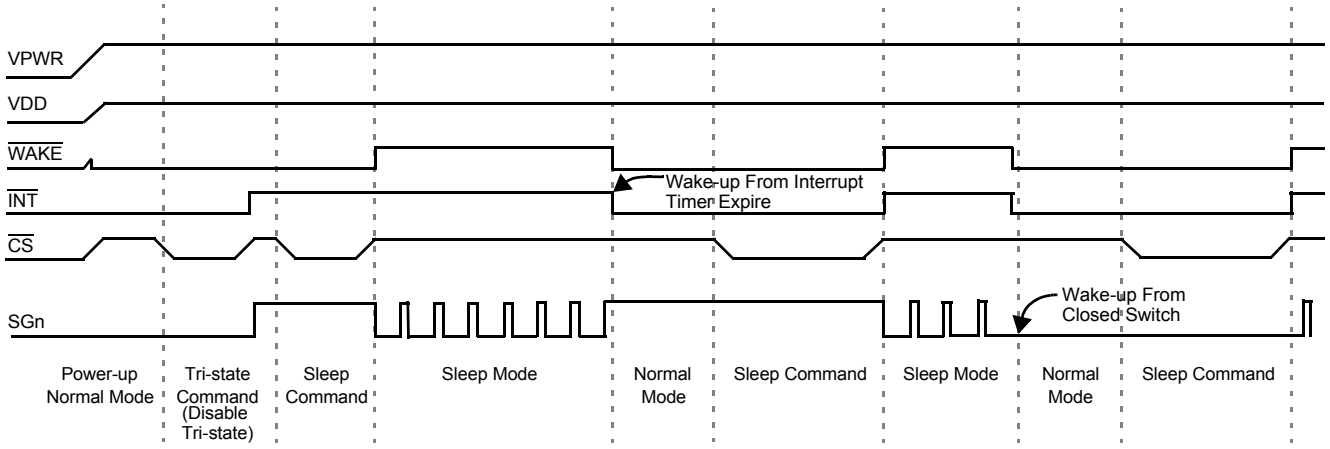


Figure 5. Sleep Mode to Normal Mode Operation

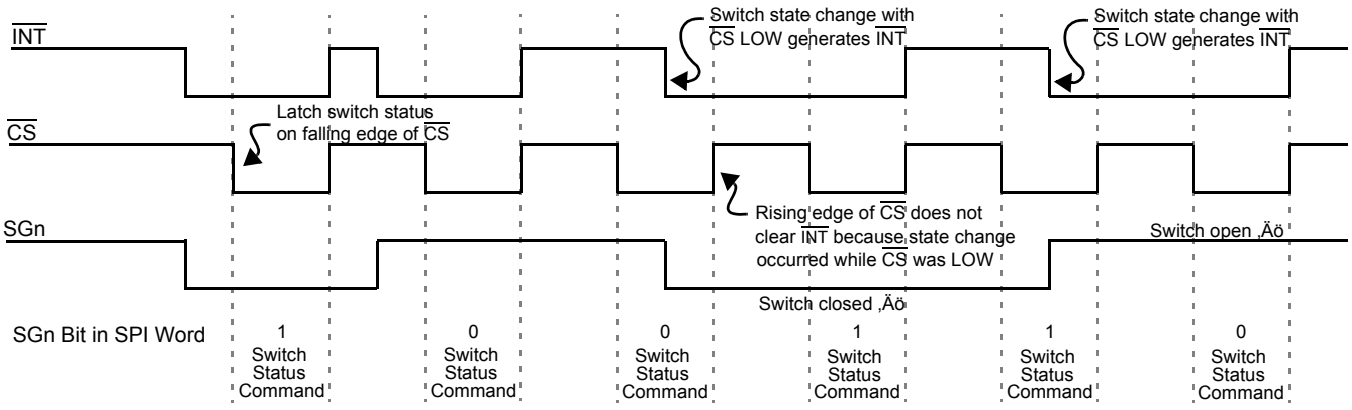


Figure 6. Normal Mode Interrupt Operation

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33972 device is an integrated circuit designed to provide systems with ultra-low quiescent sleep/wake-up modes, and a robust interface between switch contacts and a microprocessor. The 33972 replaces many of the discrete components required when interfacing to microprocessor-based systems, while providing switch ground offset protection, contact wetting current, and a system wake-up.

The 33972 features 8-programmable switch-to-ground or switch-to-battery inputs and 14 switch-to-ground inputs. All switch inputs may be read as analog inputs through the analog multiplexer (AMUX). Other features include a programmable wake-up timer, programmable interrupt timer, programmable wake-up/interrupt bits, and programmable wetting current settings.

This device is designed primarily for automotive applications, but may be used in a variety of other applications such as computer, telecommunications, and industrial controls.

FUNCTIONAL PIN DESCRIPTION

CHIP SELECT ($\overline{CS}$)

The system MCU selects the 33972 to receive communication using the chip select ($\overline{CS}$) pin. With the $\overline{CS}$ in a logic LOW state, command words may be sent to the 33972 via the serial input (SI) pin, and switch status information can be received by the MCU via the serial output (SO) pin. The falling edge of $\overline{CS}$ enables the SO output, latches the state of the $\overline{INT}$ pin, and the state of the external switch inputs.

Rising edge of the $\overline{CS}$ initiates the following operation:

1. Disables the SO driver (high-impedance)
2. $\overline{INT}$ pin is reset to logic [1], except when additional switch changes occur during $\overline{CS}$ LOW. (See Figure 6 on page 9.)
3. Activates the received command word, allowing the 33972 to act upon new data from switch inputs.

To avoid any spurious data, it is essential the HIGH-to-LOW and LOW-to-HIGH transitions of the $\overline{CS}$ signal occur only when SCLK is in a logic LOW state. A clean $\overline{CS}$ is needed to ensure no incomplete SPI words are sent to the device. Internal to the 33972 device is an active pull-up to V_{DD} on $\overline{CS}$.

In Sleep mode, the negative edge of $\overline{CS}$ (V_{DD} applied) will wake up the 33972 device. Data received from the device during $\overline{CS}$ wake-up may not be accurate.

SYSTEM CLOCK (SCLK)

The system clock (SCLK) pin clocks the internal shift register of the 33972. The SI data is latched into the input shift register on the falling edge of SCLK signal. The SO pin shifts the switch status bits out on the rising edge of SCLK. The SO data is available for the MCU to read on the falling edge of SCLK. False clocking of the shift register must be avoided to ensure validity of data. It is essential the SCLK pin be in a logic LOW state whenever $\overline{CS}$ makes any transition. For this reason, it is recommended, that the SCLK pin is commanded to a logic LOW state as long as the device is not accessed and $\overline{CS}$ is in a logic HIGH state. When the $\overline{CS}$ is in a logic HIGH state, any signal on the SCLK and SI pins will be ignored and the SO pin is tri-state.

SPI SLAVE IN (SI)

The SI pin is used for serial instruction data input. SI information is latched into the input register on the falling edge of SCLK. A logic HIGH state present on SI will program a *one* in the command word on the rising edge of the $\overline{CS}$ signal. To program a complete word, 24 bits of information must be entered into the device.

SPI SLAVE OUT (SO)

The SO pin is the output from the shift register. The SO pin remains tri-stated until the $\overline{CS}$ pin transitions to a logic LOW state. All open switches are reported as zero, all closed switches are reported as one. The negative transition of CS enables the SO driver.

The first positive transition of SCLK will make the status data bit 24 available on the SO pin. Each successive positive clock will make the next status data bit available for the MCU to read on the falling edge of SCLK. The SI/SO shifting of the data follows a first-in, first-out protocol, with both input and output words transferring the most significant bit (MSB) first.

INTERRUPT ($\overline{INT}$)

The $\overline{INT}$ pin is an interrupt output from the 33972 device. The $\overline{INT}$ pin is an open-drain output with an internal pull-up to V_{DD}. In Normal mode, a switch state change will trigger the $\overline{INT}$ pin (when enabled). The $\overline{INT}$ pin and $\overline{INT}$ bit in the SPI register are latched on the falling edge of $\overline{CS}$. This permits the MCU to determine the origin of the interrupt. When two 33972 devices are used, only the device initiating the interrupt will have the $\overline{INT}$ bit set. The $\overline{INT}$ pin is cleared on the rising edge of $\overline{CS}$. The $\overline{INT}$ pin will not clear with rising edge of $\overline{CS}$ if a switch contact change has occurred while $\overline{CS}$ was LOW.

In a multiple 33972 device system with $\overline{WAKE}$ HIGH and V_{DD} in (Sleep Mode), the falling edge of $\overline{INT}$ will place all 33972s in Normal mode.

WAKE-UP ($\overline{\text{WAKE}}$)

The $\overline{\text{WAKE}}$ pin is an open-drain output and a wake-up input. The pin is designed to control a power supply Enable pin. In the Normal mode, the $\overline{\text{WAKE}}$ pin is LOW. In the Sleep mode, the $\overline{\text{WAKE}}$ pin is HIGH. The $\overline{\text{WAKE}}$ pin has a pull-up to the internal +5.0 V supply.

In Sleep mode with the $\overline{\text{WAKE}}$ pin HIGH, the falling edge of $\overline{\text{WAKE}}$ will place the 33972 in Normal mode. In Sleep mode with V_{DD} applied, the $\overline{\text{INT}}$ pin must be HIGH for negative edge of $\overline{\text{WAKE}}$ to wake up the device. If V_{DD} is not applied to the device in Sleep mode, $\overline{\text{INT}}$ does not affect $\overline{\text{WAKE}}$ operation.

BATTERY INPUT (VPWR)

The VPWR pin is battery input and Power-ON Reset to the 33972 IC. The VPWR pin requires external reverse battery and transient protection. Maximum input voltage on VPWR is 50 V. All wetting, sustain, and internal logic current is provided from the VPWR pin.

VOLTAGE DRAIN SUPPLY (VDD)

The VDD input pin is used to determine logic levels on the microprocessor interface (SPI) pins. Current from VDD is used to drive SO output and the pull-up current for $\overline{\text{CS}}$ and $\overline{\text{INT}}$ pins. VDD must be applied for wake-up from negative edge of $\overline{\text{CS}}$ or $\overline{\text{INT}}$.

GROUND (GND)

The GND pin provides ground for the IC as well as ground for inputs programmed as switch-to-battery inputs.

PROGRAMMABLE SWITCHES (SP0:SP7)

The 33972 device has 8 switch inputs capable of being programmed to read switch-to-ground or switch-to-battery contacts. The input is compared with a 4.0 V reference. When programmed to be switch-to-battery, voltages greater than 4.0 V are considered closed. Voltages less than 4.0 V are considered open. The opposite holds true when inputs are programmed as switch-to-ground. Programming features are defined in Table 6 through Table 11 in the Functional Device Operation section of this datasheet beginning on page 13. Voltages greater than the VPWR supply voltage will source current through the SP inputs to the VPWR pin. Transient battery voltages greater than 38/40 V must be clamped by an external device. This is not a normal operating condition and can damage the IC.

SWITCH-TO-GROUND INPUTS (SG0:SG13)

The SGn pins are switch-to-ground inputs only. The input is compared with a 4.0 V reference. Voltages greater than 4.0 V are considered open. Voltages less than 4.0 V are considered closed. Programming features are defined in Table 6 through Table 11 in the Functional Device Operation section of this datasheet beginning on page 13. Voltages greater than the VPWR supply voltage will source current through the SG inputs to the VPWR pin. Transient battery voltages greater than 40 V must be clamped by an external device. This is not a normal operating condition and can damage the IC.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

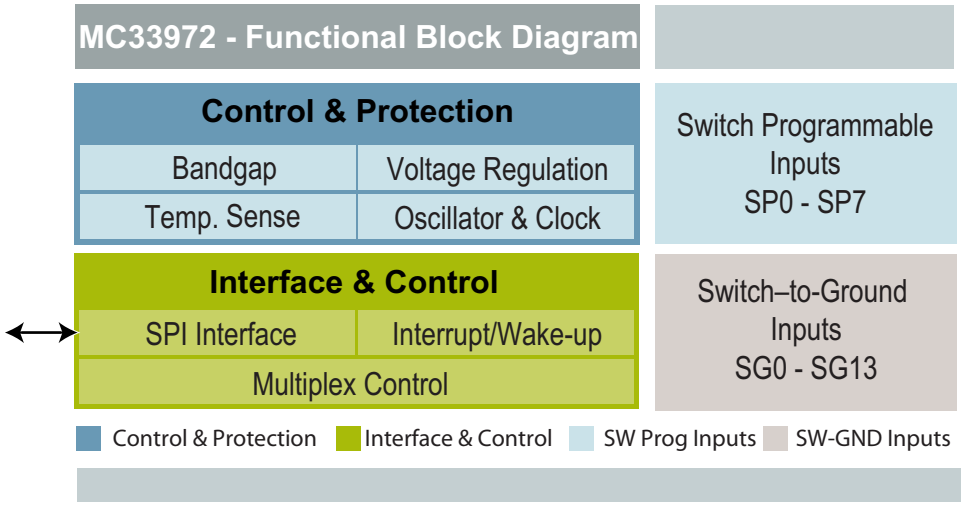


Figure 7. Functional Internal Block Description

CONTROL AND PROTECTION CIRCUITRY:

The 33972 is designed to operate from 5.5 V to 38/40 V on the VPWR terminal. Characteristics are provided for V_{PWR} from 8.0 to 26 V for the IC (parametric tests are done from 8.0 to 16.0v). Switch contact currents and the internal logic supply are generated from the VPWR terminal. The VDD supply terminal is used to set the SPI communication voltage levels, current source for the SO driver, and pull-up current on $\overline{INT}$ and $\overline{CS}$.

The on-chip voltage regulator and bandgap supplies the required voltages to the internal monitor circuitry. The temperature monitor is active in the Normal mode.

INTERFACE AND CONTROL:

The 33972 Multiple Switch Detection Interface with Suppressed Wake-up is designed to detect the closing and opening of up to 22 switch contacts. The switch status, either open or closed, is transferred to the microprocessor unit (MCU) through a serial peripheral interface (SPI).

The device also features a 22-to-1 analog multiplexer for reading inputs as analog. The 33972 device has two modes of operation, Normal and Sleep.

SWITCH PROGRAMMABLE INPUTS:

Programmable switch detection inputs. These 8 inputs can selectively detect switch closures to Ground or Battery. The 33972 device has 8 switch inputs capable of being programmed to read switch-to-ground or switch-to-battery contacts. The input is compared with a 4.0 V reference. When programmed to be switch-to-battery, voltages greater than 4.0 V are considered closed. Voltages less than 4.0 V are considered open. The opposite holds true when inputs are programmed as switch-to-ground.

SWITCH–TO-GROUND INPUTS:

Switch detection interface inputs. These 14 inputs can detect switch closures to ground only. The input is compared with a 4.0 V reference. Voltages greater than 4.0 V are considered open. Voltages less than 4.0 V are considered closed. Note: Each of these inputs may be used to supply current to sensors external to a module.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

MCU INTERFACE DESCRIPTION

The 33972 device directly interfaces to a 3.3 or 5.0 V microcontroller unit (MCU). SPI serial clock frequencies up to 6.0 MHz may be used for programming and reading switch input status (production tested at 4.16 MHz). Figure 8 illustrates the configuration between an MCU and one 33972.

Serial peripheral interface (SPI) data is sent to the 33972 device through the SI input pin. As data is being clocked into the SI pin, status information is being clocked out of the device by the SO output pin. The response to a SPI command will always return the switch status, interrupt flag, and thermal flag. Input switch states are latched into the SO register on the falling edge of the chip select ($\overline{CS}$) pin. Twenty-four bits are required to complete a transfer of information between the 33972 and the MCU.

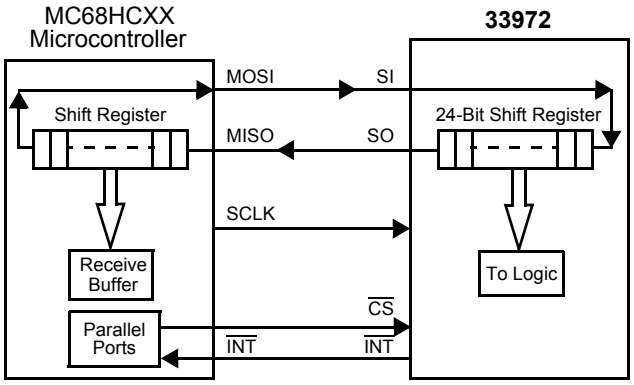


Figure 8. SPI Interface with Microprocessor

Two or more 33972 devices may be used in a module system. Multiple ICs may be SPI-configured in parallel or serial. Figures 9 and 10 show the configurations. When using the serial configuration, 48-clock cycles are required to transfer data in/out of the ICs.

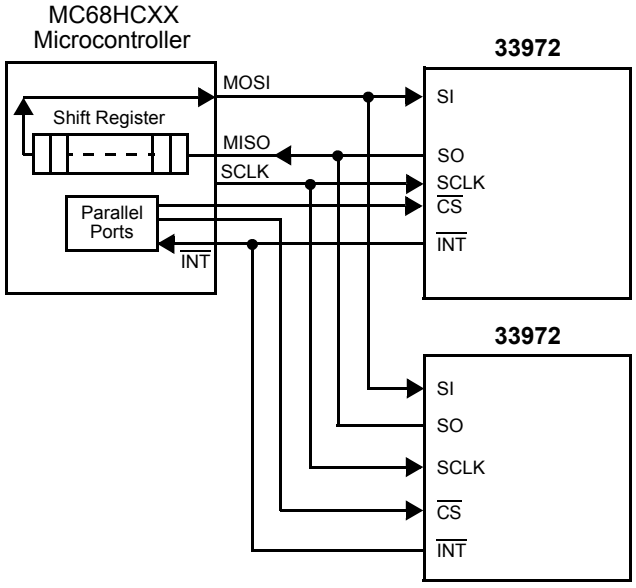


Figure 9. SPI Parallel Interface with Microprocessor

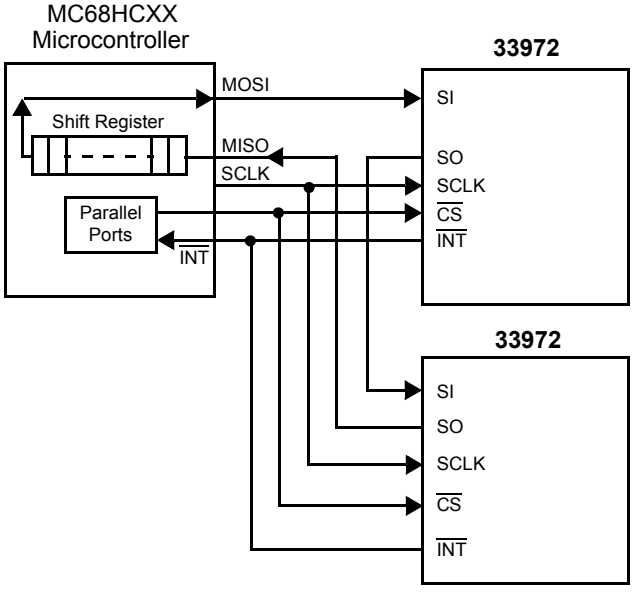


Figure 10. SPI Serial Interface with Microprocessor

POWER SUPPLY

The 33972 is designed to operate from 5.5 to 40 V on the VPWR pin. Characteristics are provided from 8.0 to 16 V for the device. Switch contact currents and the internal logic supply are generated from the VPWR pin. The VDD supply pin is used to set the SPI communication voltage levels, current source for the SO driver, and pull-up current on $\overline{INT}$ and $\overline{CS}$.

The VDD supply may be removed from the device to reduce quiescent current. If V_{DD} is removed while the device is in Normal mode, the device will remain in Normal mode. If V_{DD} is removed in Sleep mode, the device will remain in Sleep mode until a wake-up input is received ($\overline{WAKE}$ HIGH to LOW, switch input or interrupt timer expires).

Removing V_{DD} from the device disables SPI communication and will not allow the device to wake up from $\overline{INT}$ and $\overline{CS}$ pins.

POWER-ON RESET (POR)

Applying V_{PWR} to the device will cause a Power-ON Reset and place the device in Normal mode.

Default settings from Power-ON Reset via V_{PWR} or the Reset Command are as follows:

- Programmable switch – set to switch to battery
- All inputs set as wake-up
- Wetting current on (16 mA)
- Wetting current timer on (20 ms)
- All inputs tri-state
- Analog select 00000 (no input channel selected)

NORMAL AND SLEEP MODES

The 33972 has two operating modes, Normal mode and Sleep mode. A discussion on Normal mode begins below. A discussion on Sleep mode begins on page 19.

Normal Mode

Normal mode may be entered by the following events:

- Application of V_{PWR} to the IC
- Change-of-switch state (when enabled)
- Falling edge of $\overline{WAKE}$
- Falling edge of $\overline{INT}$ (with V_{DD} = 5.0 V and $\overline{WAKE}$ at Logic [1])
- Falling edge of $\overline{CS}$ (with V_{DD} = 5.0 V)
- Interrupt timer expires

Only in Normal mode with V_{DD} applied can the registers of the 33972 be programmed through the SPI.

The registers that may be programmed in Normal mode are listed below. Further explanation of each register is provided in subsequent paragraphs.

- Programmable Switch Register (*Settings Command*)
- Wake-Up/Interrupt Register (*Wake-up/Interrupt Command*)
- Wetting Current Register (*Metallic Command*)
- Wetting Current Timer Register (*Wetting Current Timer Enable Command*)
- Tri-State Register (*Tri-state Command*)
- Analog Select Register (*Analog Command*)
- Calibration of Timers (*Calibration Command*)
- Reset (*Reset Command*)

Figure 6, page 9, is a graphical description of the device operation in Normal mode. Switch states are latched into the input register on the falling edge of $\overline{CS}$. The $\overline{INT}$ to the MCU is cleared on the rising edge of $\overline{CS}$. However, $\overline{INT}$ will not clear on rising edge of $\overline{CS}$ if a switch has closed during SPI communication ($\overline{CS}$ LOW). This prevents switch states from being missed by the MCU.

PROGRAMMABLE SWITCH REGISTER

Inputs SP0 to SP7 may be programmable for switch-to-battery or switch-to-ground. These inputs types are defined using the *settings command* (Table 6). To set an SPn input for switch-to-battery, a logic [1] for the appropriate bit must be set. To set an SPn input for switch-to-ground, a logic [0] for the appropriate bit must be set. The MCU may change or update the programmable switch register via software at any time in Normal mode. Regardless of the setting, when the SPn input switch is closed a logic [1] will be placed in the serial output response register (Table 17, page 19).

Table 6. Settings Command

Settings Command								Not used								Battery/Ground Select							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0

WAKE-UP/INTERRUPT REGISTER

The wake-up/interrupt register defines the inputs that are allowed to wake the 33972 from Sleep Mode or set the $\overline{INT}$ pin LOW in Normal mode. Programming the wake-up/interrupt bit to logic [0] will disable the specific input from generating an interrupt and will disable the specific input from waking the IC in Sleep mode (Table 7). Programming the wake-up/interrupt bit to logic [1] will enable the specific input to generate an interrupt with switch change of state and will enable the specific input as wake-up. The MCU may change or update the wake-up/interrupt register via software at any time in Normal mode.

Table 7. Wake-up / Interrupt Command

Wake-up/Interrupt Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	0	0	1	1	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

WETTING CURRENT REGISTER

The 33972 has two levels of switch contact current, 16 and 2.0 mA (see Figure 11). The metallic command is used to set the switch contact current level (Table 8). Programming the metallic bit to logic [0] will set the switch wetting current to 2.0 mA. Programming the metallic bit to logic [1] will set the switch contact wetting current to 16 mA. The MCU may change or update the wetting current register via software at any time in Normal mode.

Wetting current is designed to provide higher levels of current during switch closure. The higher level of current is designed to keep switch contacts from building up oxides that form on the switch contact surface.

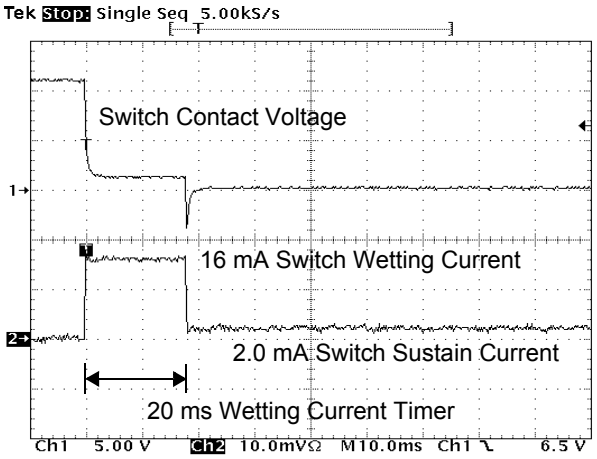


Figure 11. Contact Wetting and Sustain Current

Table 8. Metallic Command

Metallic Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	0	1	0	1	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

WETTING CURRENT TIMER REGISTER

Each switch input has a designated 20 ms timer. The timer starts when the specific switch input crosses the comparator threshold (4.0 V). When the 20 ms timer expires, the contact current is reduced from 16 to 2.0 mA. The wetting current timer may be disabled for a specific input. When the timer is disabled, 16 mA of current will continue to flow through the closed switch contact. With multiple wetting current timers disabled, power dissipation for the IC must be considered.

The MCU may change or update the wetting current timer register via software at any time in Normal mode. This allows the MCU to control the amount of time wetting current is applied to the switch contact. Programming the wetting current timer bit to logic [0] will disable the wetting current timer. Programming the wetting current timer bit to logic [1] will enable the wetting current timer (Table 9).

Table 9. Wetting Current Timer Enable Command

Wetting Current Timer Commands								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	1	0	0	0	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

TRI-STATE REGISTER

The tri-state command is use to set the SPn or SGn input node as high-impedance (Table 10). By setting the tri-state register bit to logic [1], the input will be high-impedance regardless of the metallic command setting. The comparator on each input remains active. This command allows the use of each input as a comparator with a 4.0 V threshold. The MCU may change or update the tri-state register via software at any time in Normal mode.

Table 10. Tri-State Command

Tri-State Commands								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1	X	X	X	X	X	X	X	X	sp7	sp6	sp5	sp4	sp3	sp2	sp1	sp0
0	0	0	0	1	0	1	0	X	X	sg13	sg12	sg11	sg10	sg9	sg8	sg7	sg6	sg5	sg4	sg3	sg2	sg1	sg0

ANALOG SELECT REGISTER

The analog voltage on switch inputs may be read by the MCU using the analog command (Table 11). Internal to the IC is a 22-to-1 analog multiplexer. The voltage present on the selected input pin is buffered and made available on the AMUX output pin. The AMUX output pin is clamped to a maximum of VDD volts regardless of the higher voltages present on the input pin. After an input has been selected as the analog, the corresponding bit in the next SO data stream will be logic [0]. When selecting a channel to be read as analog, the user must also set the desired current (16 mA, 2.0 mA, or high-impedance). Setting bit 6 and bit 5 to 0,0 selects the input as high-impedance. Setting bit 6 and bit 5 to 0,1 selects 2.0 mA, and 1,0 selects 16 mA. Setting bit 6 and bit 5 to 1,1 in the analog select register is not allowed and will place the input as an analog input with high-impedance.

Analog currents set by the analog command are pull-up currents for all SGn and SPn inputs (Table 11). The analog command does not allow pull-down currents on the SPn inputs. Setting the current to 16 or 2.0 mA may be useful for reading sensor inputs. Further information is provided in the Typical Applications section of this datasheet beginning on page 21. The MCU may change or update the analog select register via software at any time in Normal mode.

Table 11. Analog Command

Analog Command								Not used									Current Select		Analog Channel Select				
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	X	X	X	X	X	X	X	X	X	16 mA	2.0 mA	0	0	0	0	0

Table 12. Analog Channel

Bits 43210	Analog Channel Select
00000	No Input Selected
00001	SG0
00010	SG1
00011	SG2
00100	SG3
00101	SG4
00110	SG5
00111	SG6
01000	SG7
01001	SG8
01010	SG9
01011	SG10
01100	SG11
01101	SG12
01110	SG13
01111	SP0
10000	SP1
10001	SP2
10010	SP3
10011	SP4
10100	SP5
10101	SP6
10110	SP7

CALIBRATION OF TIMERS

In cases where an accurate time base is required, the user may calibrate the internal timers using the calibration command (Table 13). After the 33972 device receives the calibration command, the device expects 512 μs logic [0] calibration pulse on the $\overline{CS}$ pin. The pulse is used to calibrate the internal clock. No other SPI pins should transition during this 512 μs calibration pulse. Because the oscillator frequency changes with temperature, calibration is required for an accurate time base. Calibrating the timers has no affect on the quiescent current measurement. The calibration command simply makes the time base more accurate. The calibration command may be used to update the device on a periodic basis.

Table 13. Calibration Command

Calibration Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

RESET

The reset command resets all registers to Power-ON Reset (POR) state. Refer to Table 15, page 18, for POR states or the paragraph entitled Power-ON Reset (POR) on page 14 of this datasheet.

Table 14. Reset Command

Reset Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

SPI COMMAND SUMMARY

Table 15 below provides a comprehensive list of SPI commands recognized by the 33972 and the reset state of each register. Table 16 and Table 17 contain the serial output (SO) data for input voltages greater or less than the threshold level. Open switches are always indicated with a logic [0], closed switches are indicated with logic [1].

Table 15. SPI Command Summary

	MSB Command Bits								Setting Bits																LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Switch Status Command	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Settings Command Bat=1, Gnd=0 (Default state = 1)	0	0	0	0	0	0	0	1	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Wake-Up/Interrupt Bit Wake-Up=1 Non-Wake-Up=0 (Default state = 1)	0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	0	0	0	0	0	0	1	1	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Metallic Command Metallic = 1 Non-metallic = 0 (Default state = 1)	0	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	0	0	0	0	0	1	0	1	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Analog Command	0	0	0	0	0	1	1	0	X	X	X	X	X	X	X	X	X	16mA 0	2.0mA 0	0	0	0	0	0
Wetting Current Timer Enable Command Timer ON = 1 Timer OFF = 0 (Default state = 1)	0	0	0	0	0	1	1	1	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	0	0	0	0	1	0	0	0	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Tri-State Command Input Tri-State=1 Input Active = 0 (Default state = 1)	0	0	0	0	1	0	0	1	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	0	0	0	0	1	0	1	0	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Calibration Command (Default state – uncalibrated)	0	0	0	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Sleep Command (Refer to Sleep Mode on page 19.)	0	0	0	0	1	1	0	0	X	X	X	X	X	X	X	X	X	X	int timer	int timer	int timer	scan timer	scan timer	scan timer
Reset Command	0	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SO Response Will Always Send	them flg	int flg	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0

Table 16. Serial Output (SO) Bit Data

Type of Input	Input Programmed	Voltage on Input Pin	SO SPI Bit
SP	Switch to Ground	SPn < 4.0V	1
	Switch to Ground	SPn > 4.0V	0
	Switch to Battery	SPn < 4.0V	0
	Switch to Battery	SPn > 4.0V	1
SG	N/A	SGn < 4.0V	1
	N/A	SGn > 4.0V	0

Table 17. Serial Output (SO) Response Register

SO Response Will Always Send	them flg	int flg	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0

EXAMPLE OF NORMAL MODE OPERATION

The operation of the device in Normal mode is defined by the states of the programmable internal control registers. A typical application may have the following settings:

- Programmable switch – set to switch-to-ground
- All inputs set as wake-up
- Wetting current on (16 mA)
- Wetting current timer on (20 ms)
- All inputs tri-state-disabled (comparator is active)
- Analog select 00000 (no input channel selected)

With the device programmed as above, an interrupt will be generated with each switch contact change of state (open-to-close or close-to-open) and 16 mA of contact wetting current will be source for 20 ms. The $\overline{INT}$ pin will remain LOW until switch status is acknowledged by the microprocessor. It is critical to understand $\overline{INT}$ will not be cleared on the rising edge of $\overline{CS}$ if a switch closure occurs while $\overline{CS}$ is LOW. The maximum duration a switch state change can exist without acknowledgement depends on the software response time to the interrupt. Figure 6, page 9, shows the interaction between changing input states and the $\overline{INT}$ and $\overline{CS}$ pins.

If desired the user may disable interrupts (wake up/ interrupt command) from the 33972 device and read the switch states on a periodic basis. Switch activation and deactivation faster than the MCU read rate will not be acknowledged.

The 33972 device will exit the Normal mode and enter the Sleep mode only with a valid sleep command.

SLEEP MODE

Sleep mode is used to reduce system quiescent currents. Sleep mode may be entered only by sending the sleep command. All register settings programmed in Normal mode will be maintained in Sleep mode.

The 33972 will exit Sleep mode and enter Normal mode when any of the following events occur:

- Input switch change of state (when enabled)
- Interrupt timer expire
- Falling edge of $\overline{WAKE}$
- Falling edge of $\overline{INT}$ (with V_{DD} = 5.0 V and $\overline{WAKE}$ at Logic [1])
- Falling edge of $\overline{CS}$ (with V_{DD} = 5.0 V)
- Power-ON Reset (POR)

The V_{DD} supply may be removed from the device during Sleep mode. However removing V_{DD} from the device in Sleep mode will disable a wake-up from falling edge of $\overline{INT}$ and $\overline{CS}$.

Note In cases where $\overline{CS}$ is used to wake the device, the first SO data message is not valid.

The sleep command contains settings for two programmable timers for Sleep mode, the interrupt timer and the scan timer, as shown in Table 18 The interrupt timer is used as a periodic wake-up timer. When the timer expires, an interrupt is generated and the device enters Normal mode.

Note The interrupt timer in the 33972 device may be disabled by programming the interrupt bits to logic [1 1 1].

Table 19 shows the programmable settings of the Interrupt timer.

Table 18. Sleep Command

Sleep Command								Command Bits															
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	X	X	X	X	X	X	X	X	X	X	int timer	int timer	int timer	scan timer	scan timer	scan timer

Table 19. Interrupt Timer

Bits 543	Interrupt Period
000	32 ms
001	64 ms
010	128 ms
011	256 ms
100	512 ms
101	1.024 s
110	2.048 s
111	No interrupt wake-up

The scan timer sets the polling period between input switch reads in Sleep mode. The period is set in the sleep command and may be set to 000 (no period) to 111 (64 ms). In Sleep mode when the scan timer expires, inputs will behave as programmed prior to sleep command. The 33972 will wake up for approximately 125 μs and read the switch inputs. At the end of the 125 μs, the input switch states are compared with the switch state prior to sleep command. When switch state changes are detected, an interrupt is generated (when enabled; refer to wake-up/interrupt command description on page 15), and the device enters Normal mode. Without switch state changes, the 33972 will reset the scan timer, inputs become tri-state, and the Sleep mode continues until the scan timer expires again.

Table 20 shows the programmable settings of the Scan timer.

Table 20. Scan Timer

Bits 210	Scan Period
000	No Scan
001	1.0 ms
010	2.0 ms
011	4.0 ms
100	8.0 ms
101	16 ms
110	32 ms
111	64 ms

Note The interrupt and scan timers are disabled in the Normal Mode.

Figure 5, page 9, is a graphical description of how the 33972 device exits Sleep mode and enters Normal mode. Notice that the device will exit Sleep mode when the interrupt timer expires or when a switch change of state occurs. The falling edge of $\overline{INT}$ triggers the MCU to wake from Sleep state. Figure 12 illustrates the current consumed during Sleep mode. During the 125 μs, the device is fully active and switch states are read. The quiescent current is calculated by integrating the normal running current over scan period plus approximately 60 μA.

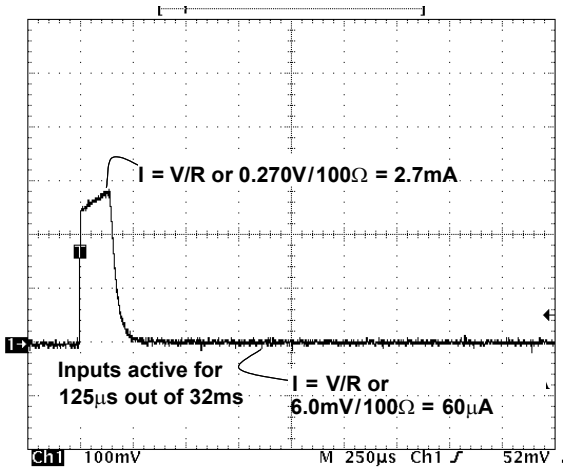


Figure 12. Sleep Current Waveform

TEMPERATURE MONITOR

With multiple switch inputs closed and the device programmed with the wetting current timers disabled, considerable power will be dissipated by the IC. For this reason, temperature monitoring has been implemented. The temperature monitor is active in the Normal mode only. When the IC temperature is above the thermal limit, the temperature monitor will do all of the following:

- Generate an interrupt.
- Force all 16 mA pull-up and pull-down current sources to revert to 2.0 mA current sources.
- Maintain the 2.0 mA current source and all other functionality.
- Set the thermal flag bit in the SPI output register.

The thermal flag bit in the SPI word will be cleared on rising edge of $\overline{CS}$ provided the die temperature has cooled below the thermal limit. When die temperature has cooled below thermal limit, the device will resume previously programmed settings.

TYPICAL APPLICATIONS

INTRODUCTION

The 33972's primary function is the detection of open or closed switch contacts. However, there are many features that allow the device to be used in a variety of applications. The following is a list of applications to consider for the IC:

Sensor Power Supply

Switch Monitor for Metallic or Elastomeric Switches

Analog Sensor Inputs (Ratiometric)

Power MOSFET/LED Driver and Monitor

Multiple 33972 Devices in a Module System

The following paragraphs describe the applications in detail.

SENSOR POWER SUPPLY

Each input may be used to supply current to sensors external to a module. Many sensors such as Hall effect, pressure sensors, and temperature sensors require a supply voltage to power the sensor and provide an open collector or analog output. Figure 13 shows how the 33972 may be used to supply power and interface to these types of sensors. In an application where the input makes continuous transitions, consider using the wake-up/interrupt command to disable the interrupt for the particular input.

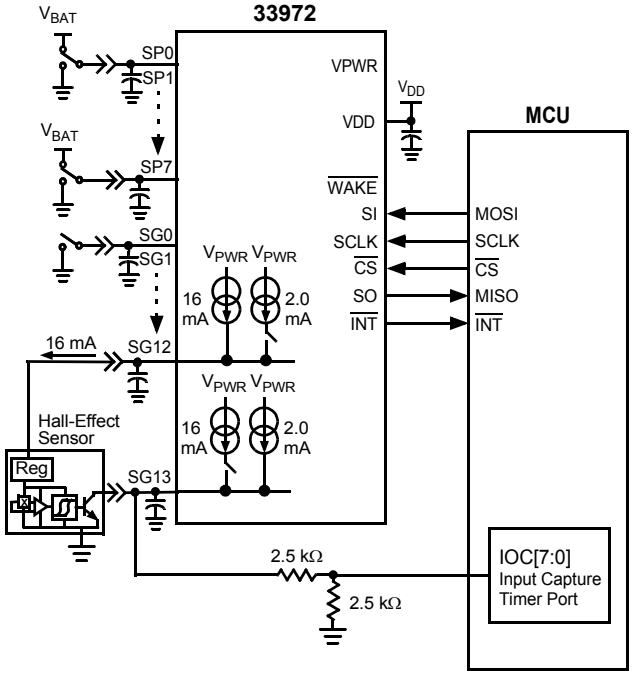


Figure 13. Sensor Power Supply

METALLIC/ELASTOMERIC SWITCH

Metallic switch contacts often develop higher contact resistance over time owing to contact corrosion. The corrosion is induced by humidity, salt, and other elements that exist in the environment. For this reason the 33972 provides two settings for contacts. When programmed for metallic switches, the device provides higher wetting current to keep switch contacts free of oxides. The higher current occurs for the first 20 ms of switch closure. Where longer duration of wetting current is desired, the user may send the wetting current timer command and disable the timer. Wetting current will be continuous to the closed switch. After the time period set by the MCU, the wetting current timer command may be sent again to enable the timer. The user must consider power dissipation on the device when disabling the timer. (Refer to the paragraph entitled Temperature Monitor, page 20.)

To increase the amount of wetting current for a switch contact, the user has two options. Higher wetting current to a switch may be achieved by paralleling SGn or SPn inputs. This will increase wetting current by 16 mA for each input added to the switch contact. The second option is to simply add an external resistor pull-up to the V_{PWR} supply for switch-to-ground inputs or a resistor to ground for a switch-to-battery input. Adding an external resistor has no effect on the operation of the device.

Elastomeric switch contacts are made of carbon and have a high contact resistance. Resistance of 1.0 kΩ is common. In applications with elastomeric switches, the pull-up and pulldown currents must be reduced to prevent excessive power dissipation at the contact. Programming for a lower current settings is provided in the Functional Device Operation section beginning on page 13 under Table 8, Metallic Command.

ANALOG SENSOR INPUTS (RATIOMETRIC)

The 33972 features a 22-to-1 analog multiplexer. Setting the binary code for a specific input in the analog command allows the microcontroller to perform analog to digital conversion on any of the 22 inputs. On rising edge of CS the multiplexer connects a requested input to the AMUX pin. The AMUX pin is clamped to max of VDD volts regardless of the higher voltages present on the input pin. After an input has been selected as the analog, the corresponding bit in the next SO data stream will be logic [0].

The input pin, when selected as analog, may be configured as analog with high-impedance, analog with 2.0 mA pull-up, or analog with 16 mA pull-up. Figure 14, page 22, shows how the 33972 may be used to provide a ratiometric reading of variable resistive input.

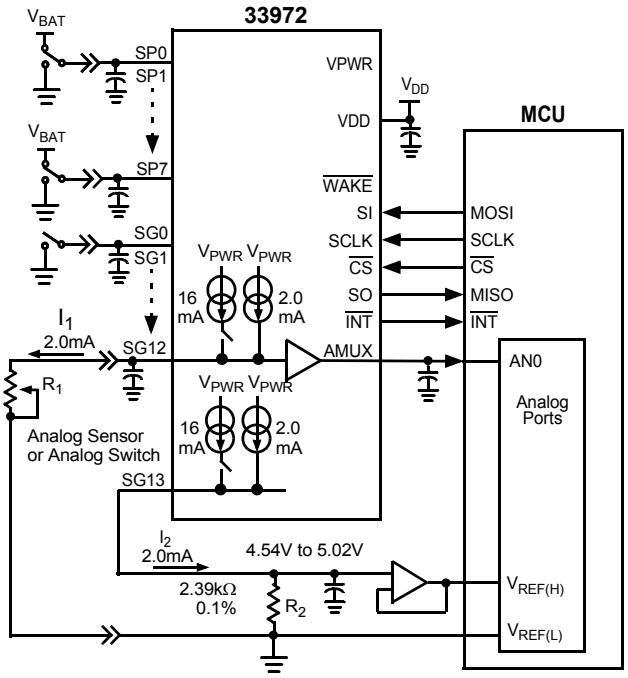


Figure 14. Analog Ratiometric Conversion

To read a potentiometer sensor, the wiper should be grounded and brought back to the module ground, as illustrated in Figure 14. With the wiper changing the impedance of the sensor, the analog voltage on the input will represent the position of the sensor.

Using the Analog feature to provide 2.0 mA of pull-up current to an analog sensor may induce error due to the accuracy of the current source. For this reason, a ratiometric conversion must be considered. Using two current sources (one for the sensor and one to set the reference voltage to the A/D converter) will yield a maximum error (owing to the 33972) of 4%.

Higher accuracy may be achieved through module level calibration. In this example, we use the resistor values from Figure 14 and assume the current sources are 4% from each other. The user may use the module end-of-line tester to calculate the error in the A/D conversion. By placing a 2.0 kΩ, 0.1% resistor in the end-of-line test equipment and assuming a perfect 2.0 mA current source from the 33972, a calculated A/D conversion may be obtained. Using the equation yields the following:

$$ADC = \frac{I1 \times R1}{I2 \times R2} \times 255$$

$$ADC = \frac{2.0mA \times 2.0k\Omega}{2.0mA \times 2.39k\Omega} \times 255$$

$$ADC = 213 \text{ counts}$$

The ADC value of 213 counts is the value with 0% error (neglecting the resistor tolerance and AMUX input offset voltage). Now we can calculate the count value induced by the mismatch in current sources. From a sample device the maximum current source was measured at 2.05 mA and minimum current source was measured at 1.99 mA. This yields 3% error in A/D conversion. The A/D measurement will be as follows:

$$ADC = \frac{1.99mA \times 2.0k\Omega}{2.05mA \times 2.39k\Omega} \times 255$$

$$ADC = 207 \text{ counts}$$

This A/D conversion is 3% low in value. The error correction factor of 1.03 may be used to correct the value:

$$ADC = 207 \text{ counts} \times 1.03$$

$$ADC = 213 \text{ counts}$$

An error correction factor may then be stored in E^2 memory and used in the A/D calculation for the specific input. Each input used as analog measurement will have a dedicated calibrated error correction factor.

POWER MOSFET/LED DRIVER AND MONITOR

Because of the flexible programming of the 33972 device, it may be used to drive small loads like LEDs or MOSFET gates. It was specifically designed to power up in the Normal mode with the inputs tri-state. This was done to ensure the LEDs or MOSFETs connected to the 33972 power up in the off-state. The switch programmable inputs (SP0–SP7) have a source-and-sink capability, providing effective MOSFET gate control. To complete the circuit, a pull-down resistor should be used to keep the gate from floating during the Sleep modes. Figure 15, page 23, shows an application where the SG0 input is used to monitor the drain-to-source voltage of the external MOSFET. The 1.5 kΩ resistor is used to set the drain-to-source trip voltage. With the 2.0 mA current source enabled, an interrupt will be generated when the drain-to-source voltage is approximately 1.0 V.

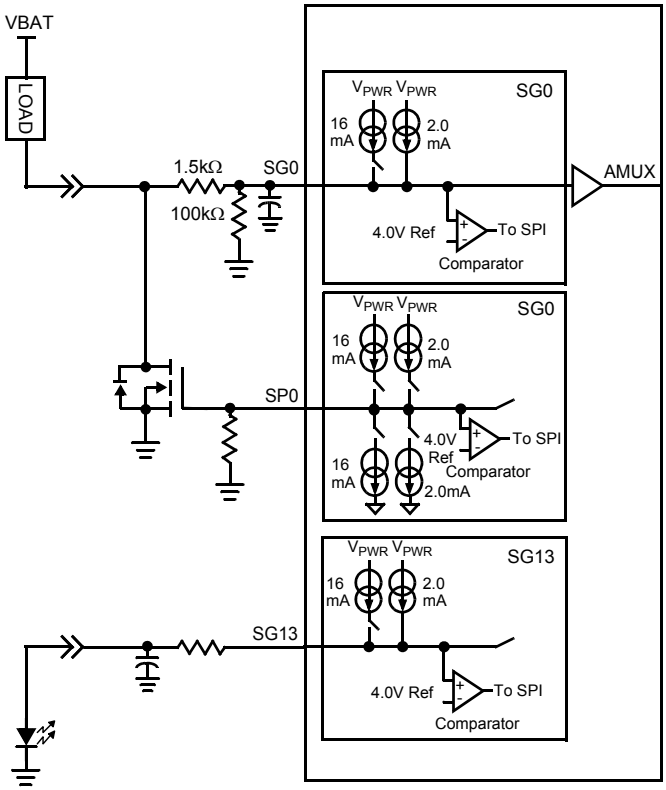


Figure 15. MOSFET or LED Driver Output

The sequence of commands (from Normal mode with inputs tri-state) required to set up the device to drive a MOSFET are as follows:

- wetting current timer enable command – Disable SPn wetting current timer (refer to Table 9, page 15).
- metallic command – Set SPn to 16 or 2.0 mA gate drive current (refer to Table 8, page 15).
- settings command – Set SPn as switch-to-battery (refer to Table 6, page 14).
- tri-state command – Disable tri-state for SPn (refer to Table 10, page 16).

After the tri-state command has been sent (tri-state disable), the MOSFET gate will be pulled to ground. From this point forward the MOSFET may be turned on and off by sending the settings command:

- settings command – SPn as switch-to-ground (MOSFET ON).
- settings command – SPn as switch-to-battery (MOSFET OFF).

Monitoring of the MOSFET drain in the OFF state provides open load detection. This is done by using an SGn input comparator. With the SGn input in tri-state, the load will pull up the SGn input to battery. With open load the SGn pin is pulled down to ground through an external resistor. The open load is indicated by a logic [1] in the SO data bit.

The analog command may be used to monitor the drain voltage in the MOSFET ON state. By sourcing 2.0 mA of current to the 1.5 kΩ resistor, the analog voltage on the SGn pin will be approximately:

$$V_{SGn} = I_{SGn} \times 1.5k\Omega + V_{DS}$$

As the voltage on the drain of the MOSFET increases, so does the voltage on the SGn pin. With the SGn pin selected as analog, the MCU may perform the A/D conversion.

Using this method for controlling unclamped inductive loads is not recommended. Inductive flyback voltages greater than V_{PWR} may damage the IC.

The SP0:SP7 pins of this device may also be used to send signals from one module to another. Operation is similar to the gate control of a MOSFET.

- For LED applications a resistor in series with the LED is recommended but not required. The switch-to-ground inputs are recommended for LED application. To drive the LED use the following commands:
- wetting current timer enable command – Disable SGn wetting current timer.
- metallic command – Set SGn to 16 mA.

From this point forward the LED may be turned on and off using the tri-state command:

- tri-state command – Disable tri-state for SGn (LED ON).
- tri-state command – Enable tri-state for SGn (LED OFF).

These parameters are easily programmed via SPI commands in Normal mode.

MULTIPLE 33972 DEVICES IN A MODULE SYSTEM

Connecting power to the 33972 and the MCU for Sleep mode operation may be done in several ways. Table 21 shows several system configurations for power between the MCU and the 33972 and their specific requirements for functionality.

Table 21. Sleep Mode Power Supply

MCU V_{DD}	33972 V_{DD}	Comments
5.0 V	5.0 V	All wake-up conditions apply. (Refer to Sleep Mode, page 19.)
5.0 V	0 V	SPI wake-up is not possible.
0 V	5.0 V	Sleep mode not possible. Current from $\overline{CS}$ pull-up will flow through MCU to V_{DD} that has been switched off. Negative edge of $\overline{CS}$ will put 33972 in Normal mode.
0 V	0 V	SPI wake-up is not possible.

Multiple 33972 devices may be used in a module system. SPI control may be done in parallel or serial. However when parallel mode is used, each device is addressed independently (refer to MCU Interface Description, page 13). Therefore when sending the sleep command, one device will enter sleep before the other. For multiple devices in a system, it is recommended that the devices are controlled in serial (S0

from first device is connected to SI of second device). With two devices, 48 clock pulses are required to shift data in. When the $\overline{\text{WAKE}}$ feature is used to enable the power supply, both $\overline{\text{WAKE}}$ pins should be connected to the enable pin on the power supply. The $\overline{\text{INT}}$ pins may be connected to one interrupt pin on the MCU or may have their own dedicated interrupt to the MCU.

The transition from Normal to Sleep mode is done by sending the sleep command. With the devices connected in serial and the sleep command sent, both will enter Sleep mode on the rising edge of $\overline{\text{CS}}$. When Sleep mode is entered, the $\overline{\text{WAKE}}$ pin will be logic [1]. If either device wakes up, the $\overline{\text{WAKE}}$ pin will transition LOW, waking the other device.

A condition exists where the MCU is sending the sleep command (CS logic [0]) and a switch input changes state. With this event the device that detects this input will not transition to Sleep mode, while the second device will enter Sleep mode. In this case two switch status commands must be sent to receive accurate switch status data. The first switch status command will wake the device in Sleep mode. Switch status data may not be valid from the first switch status command because of the time required for the input voltage to rise above the 4.0 V input comparator threshold. This time is dependant on the impedance of SGn or SPn node. The second switch status command will provide accurate switch status information. It is recommended that software wait 10 to 20 ms between the two switch status commands, allowing time for switch input voltages to stabilize. With all switch states acknowledged by the MCU, the sleep sequence may be initiated. All parameters for Sleep mode should be updated prior to sending the sleep command.

The 33972 IC has an internal 5.0 V supply from the VPWR pin. A POR circuit monitors the internal 5.0 V supply. In the event of transients on the VPWR pin, an internal reset may occur. Upon reset the 33972 will enter Normal mode with the internal registers as defined in Table 15, page 18. Therefore it is recommended that the MCU periodically update all registers internal to the IC.

USING THE $\overline{\text{WAKE}}$ FEATURE

The 33972 provides a $\overline{\text{WAKE}}$ output and wake-up input designed to control an enable pin on system power supply. While in the Normal mode, the $\overline{\text{WAKE}}$ output is LOW, enabling the power supply. In the Sleep mode, the $\overline{\text{WAKE}}$ pin is high, disabling the power supply. The $\overline{\text{WAKE}}$ pin has a passive pull-up to the internal 5.0 V supply but may be pulled up through a resistor to the V_{PWR} supply (see Figure 17, page 25)

When the $\overline{\text{WAKE}}$ output is not used, the pin should be pulled up to the V_{DD} supply through a resistor as shown in Figure 16, page 25.

During the Sleep mode, a switch closure will set the $\overline{\text{WAKE}}$ pin LOW, causing the 33972 to enter the Normal mode. The power supply will then be activated, supplying power to the VDD pin and the microprocessor and the 33972. The microprocessor can determine the source of the wake-up by reading the interrupt flag.

COST AND FLEXIBILITY

Systems requiring a significant number of switch interfaces have many discrete components. Discrete components on standard PWB consume board space and must be checked for solder joint integrity. An integrated approach reduces solder joints, consumes less board space, and offers wider operating voltage, analog interface capability, and greater interfacing flexibility.

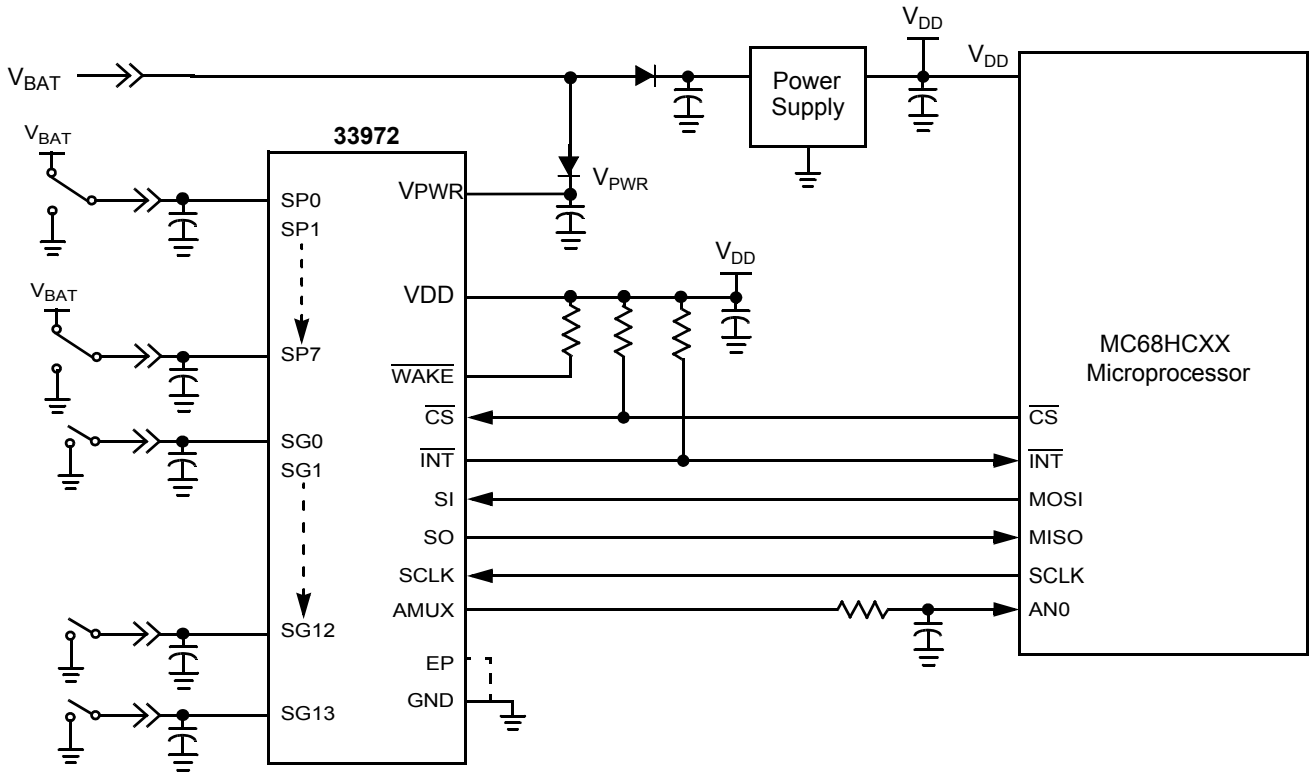


Figure 16. Power Supply Active in Sleep Mode

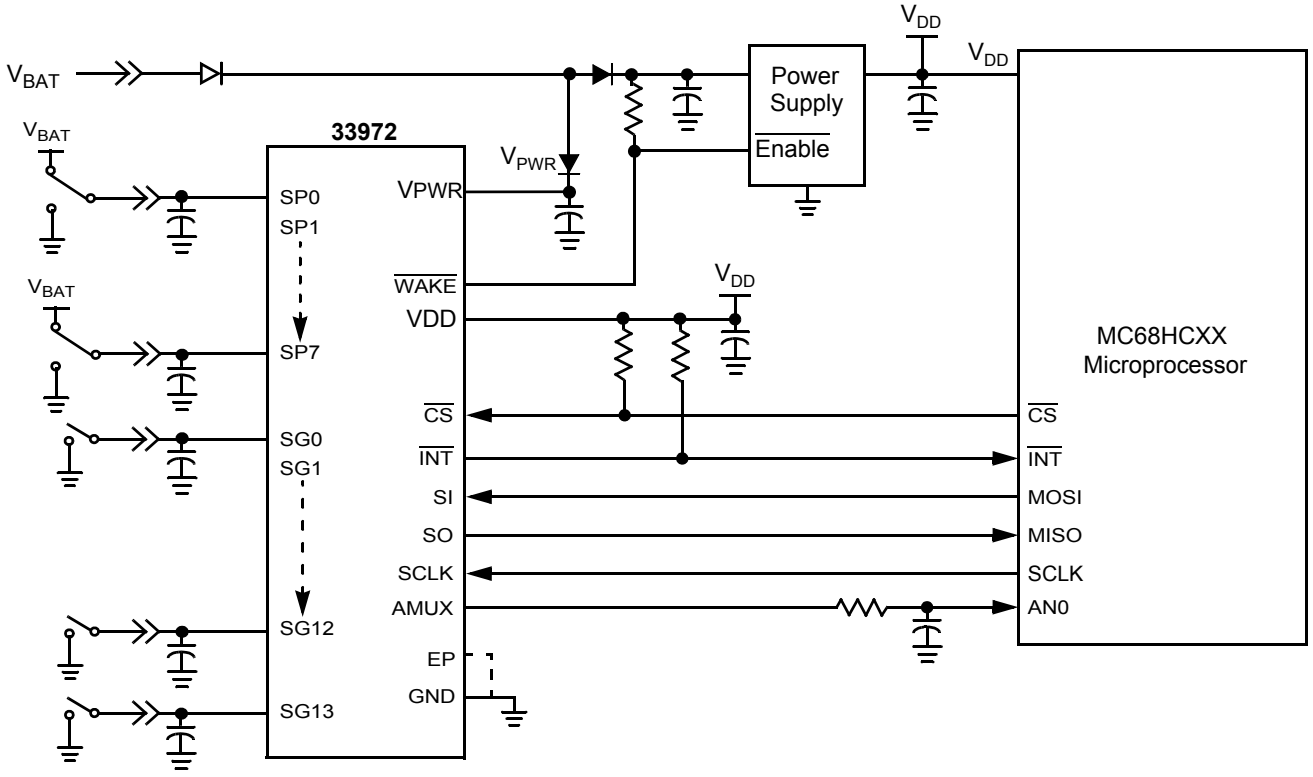
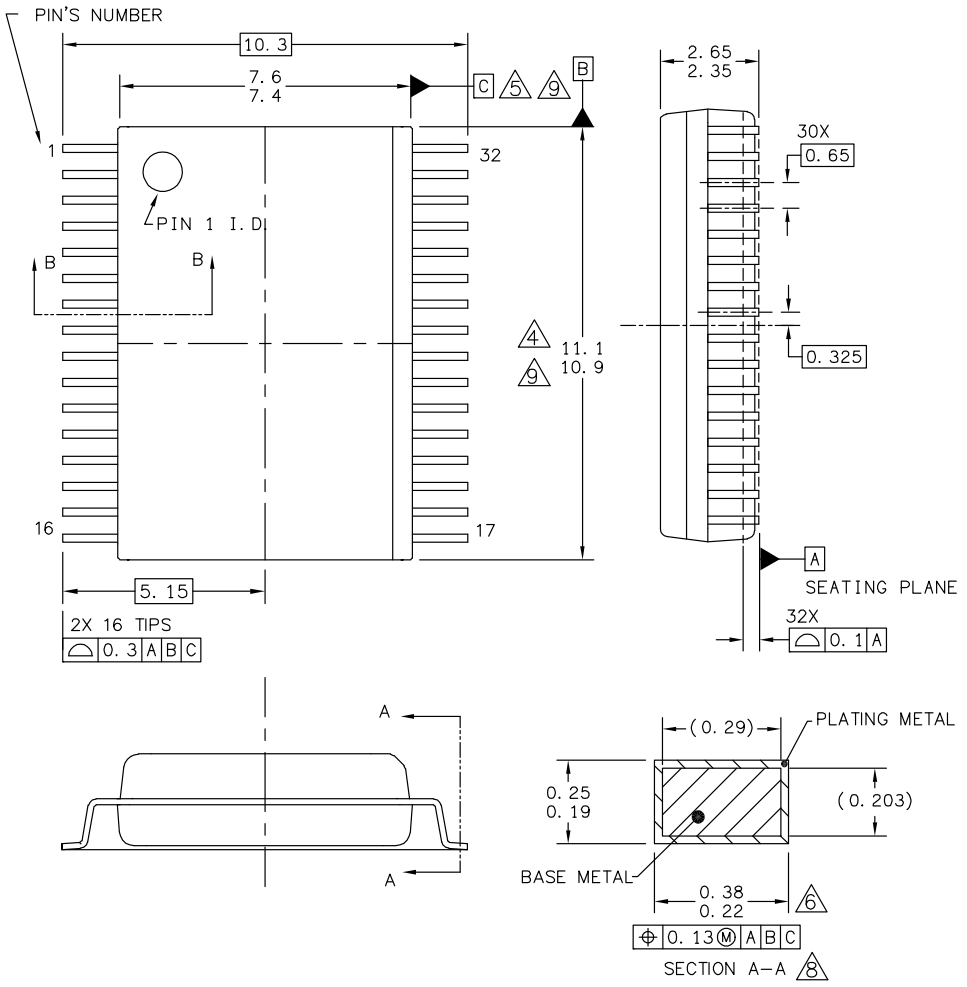


Figure 17. Power Supply Shutdown in Sleep Mode

PACKAGING

PACKAGE DIMENSIONS

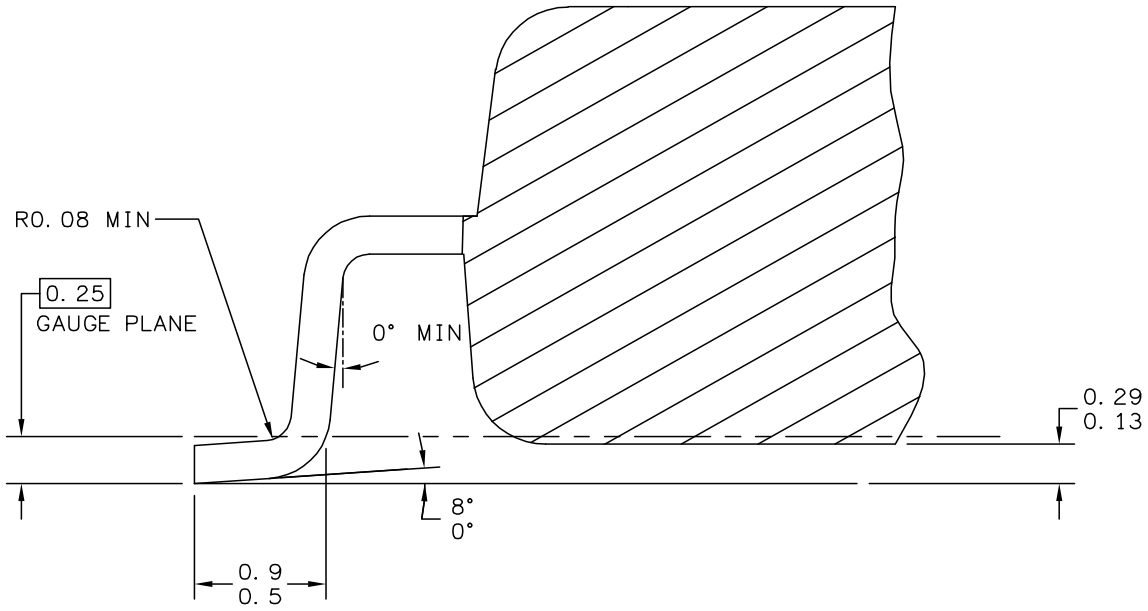
For the most current package revision, visit **www.freescale.com** and perform a keyword search using the 98A listed below.



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	CASE NUMBER: 1324–03	07 APR 2005
	STANDARD: FREESCALE	

EW SUFFIX (Pb-FREE)
32-LEAD SOIC WIDE BODY
98ARH99137A
ISSUE B

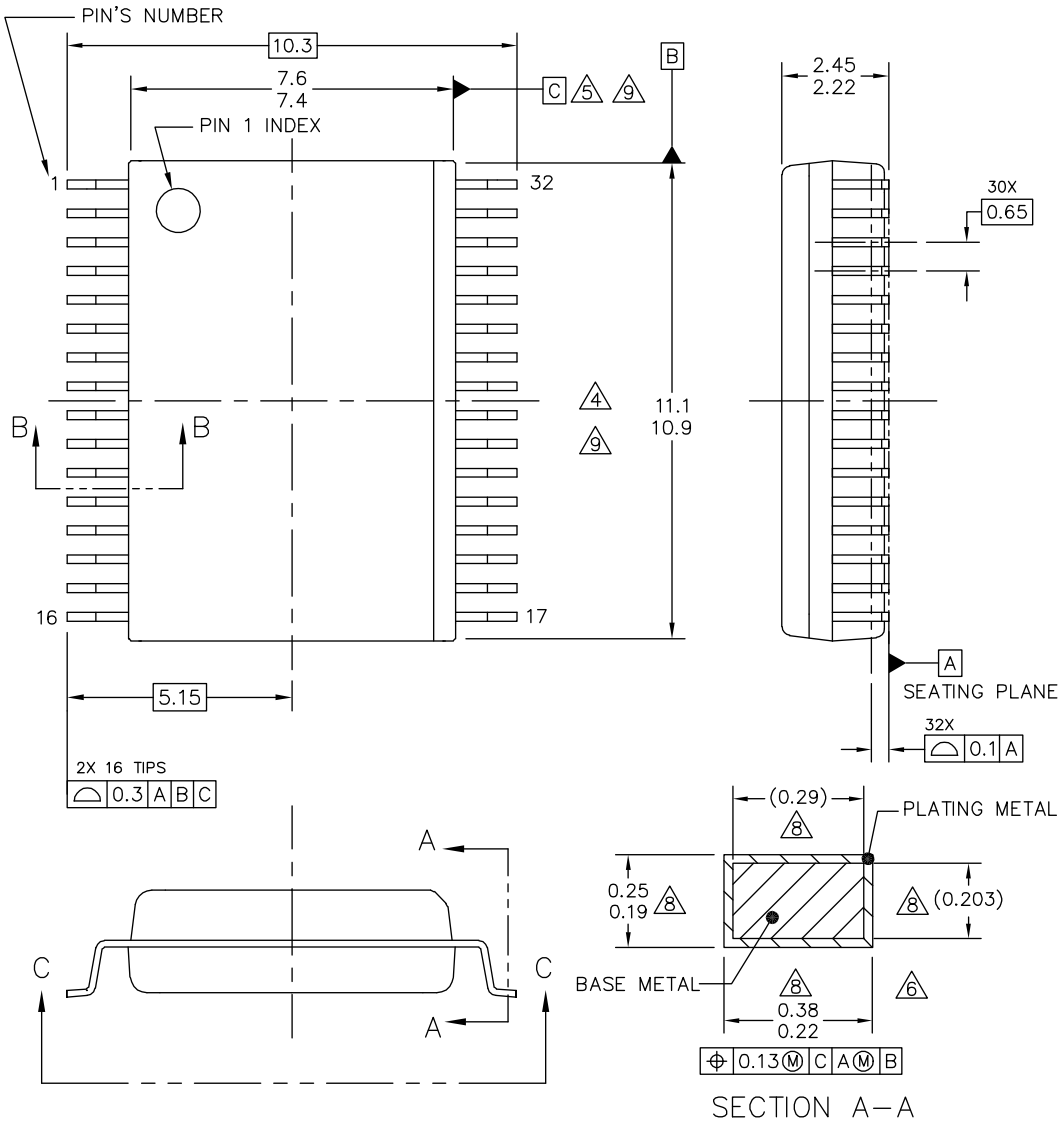
PACKAGE DIMENSIONS (CONTINUED)



SECTION B–B

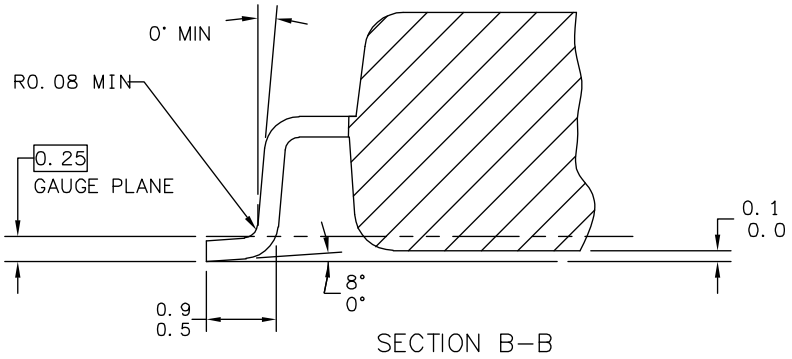
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	STANDARD: FREESCALE	

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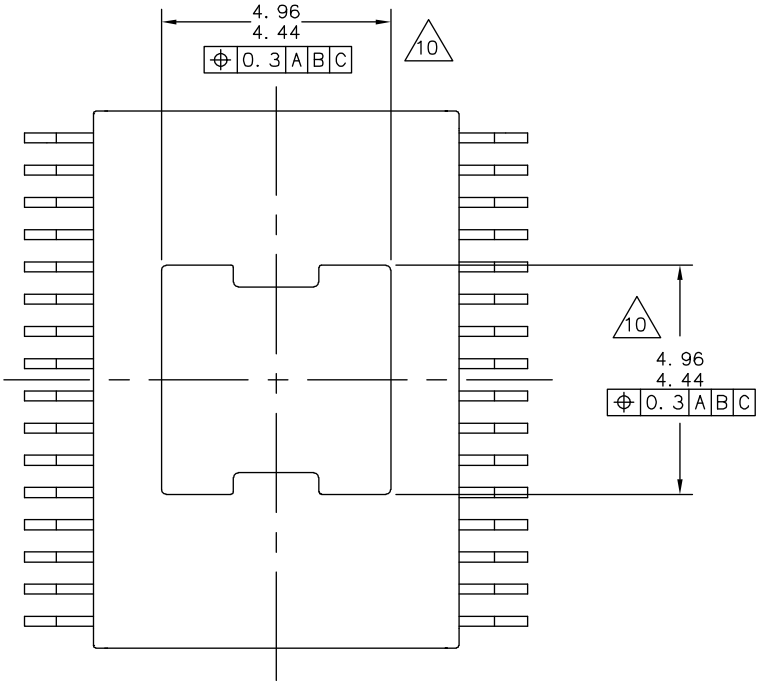


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SECTION B–B



VIEW C–C

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EXPOSED PAD
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ISSUE D

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSION RANGES DEFINE THE PRIMARY KEEP–OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.34mm FROM MAXIMUM EXPOSED PAD SIZE

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ISSUE D

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
4.0	2/2006	• Converted to Freescale format • Added PC33972A version • Changed Figure 15, Power Supply Active in Sleep Mode • Changed Figure 16, Power Supply Shutdown in Sleep Mode • Updated Outline Drawing for package
5.0	6/2006	• Update to the prevailing Freescale form and style.
6.0	7/2006	• Added MC33972T devices. • Updated StatiC Electrical Characteristics on page 6 with 33972T parameters.
7.0	11/2006	• Changed Human Body Model parameters in Maximum Ratings table. • Replaced Part Number MC33972TEW/R2 with MCZ33972TEW/R2 • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 5. Added note with instructions to obtain this information from www.freescale.com.
8.0	12/2006	• Restated note (6) • Changed Part Number MCZ33972TEW/R2 with MC33972TEW/R2
9.0	4/2007	• Removed all references to the 33972T device. • Removed the MC33972TDWB/R2, MC33972TEW/R2, and PC33972AEW/R2 from the ordering information. • Added MCZ33972AEW/R2 to the ordering information.
10.0	6/2007	• Added MC33972EW/R2, MC33972TDWB/R2, MC33972TEW/R2, and MCZ33972TEW/R2 to the ordering information.
11.0	11/2007	• Updated to the current Freescale form and style • Added MC33972AEK/R2 to the ordering information. • Included device specific information relevant to the EK suffix on pages 1, 2, 4, 5, 6, 27, and 28. • Added sentence to CHIP SELECT (CS) on page 10 • Made calculation corrections to Analog Sensor Inputs (Ratiometric)
12.0	12/2007	• Corrected Device Variation Table on page 2.
13.0	12/2007	• Replaced Outline Drawing 98ARL10543D with 98ASA10556D.
14.0	6/2008	• Added Note 7, “T_C is the T_{CASE} of the package” to Electrical Characteristics Table.
15.0	8/2008	• Updated package drawing 98ASA10556D
16.0	10/2009	• Updated data sheet status from Advance Information to Technical Data • Updated to the current Freescale form and style
17.0	2/2011	• Updated Freescale form and style • Added RoHS symbol
18.0	8/2011	• Revised Ordering Information Table by adding part numbers MC33972AEK/R2 and MC33972ATEW/R2, and removing part numbers MC33972DWB/R2 and MC33972TDWB/R2.
19.0	3/2012	• Added the sentence “This condition in not a normal operating condition and can cause damage to the IC.” to Programmable Switches (SP0:SP7) and Switch-to-ground Inputs (SG0:SG13) • Changed sentence in Control and Protection Circuitry: “Characteristics are provided for V_{PWR} from 8.0v to 26v for the IC (parametric tests are done from 8.0v to 16.0v).”

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